

**Amendment to the Specification**

Please replace paragraph [0001] with the following paragraph:

--This application is a continuation of prior application Serial No. 10/322,595, filed December 19, 2002, now ~~allowed~~; U.S. Patent No. 6,738,110, which claims priority to Korean Patent Application No. 2001-87522, filed on December 28, 2001, each of which are hereby incorporated by reference for all purposes as if fully set forth herein.--

Please replace paragraph [0006] with the following paragraph:

A typical driving method of a pixel will be described hereinafter with reference to FIG. 2 which is a signal graph illustrating voltage signals of a gate electrode and a common electrode during a frame. The graph shows applying states of a gate voltage ( $V_g$ ) and a common voltage ( $V_{com}$ ) during a frame period. In FIG. 2,  $V_{gh}$  and  $V_{gl}$  show a high and a low state of the gate voltage  $V_g$  and  $V_{dh}$ ,  $V_{dl}$  respectively, and  $V_{dl}$  show a high and a low state of the data voltage  $V_d$ . As shown in the figure, a voltage of about +18 volts is applied when the gate voltage ( $V_g$ ) is in the on state and a voltage of about 5 volts is applied when the gate voltage ( $V_g$ ) is in an off state. A high-level data voltage ( $V_d$ ) is ~~inputted~~input when the gate voltage ( $V_g$ ) is in the on state and maintained until a next gate voltage ( $V_g$ ) reaches the on state. This voltage applying process fulfills a drive of liquid crystal in the pixel region. If the liquid crystal display (LCD) device is normally black mode, a black color is displayed when the voltage is not applied. However, a light leakage phenomenon occurs in region "A" of FIG. 1 when the gate voltage ( $V_g$ ) is in the off state.

Please replace paragraph [0008] with the following paragraph:

In FIG. 3, region "B" shows an electric field distribution in a region "E" between the gate electrode 14 and the common electrode 17. In FIG. 4, region "F" is a long axis direction of the liquid crystal 19 and region "D" is a rubbing direction of a substrate. As shown in FIG. 4, the liquid crystal 19 is aligned parallel with the rubbing direction when the voltage is not applied. However, an electric potential difference ~~actual~~actually exists in the region "A" between the gate electrode 14 and the common electrode 17. Subsequently, the electric field

distribution occurs, which has a certain direction, between the gate electrode 14 and the common electrode 17. As shown in FIG. 3 and FIG. 4, the electric field direction is perpendicular to the long axes "F" of the liquid crystal 19 in the region between the gate electrode 14 and the common electrode 17. The liquid crystal 19 will subsequently align according to the electric field direction when the gate voltage ( $V_g$ ) is in the off state. Accordingly, light irradiated from a backlight passes through the "A" region and thus the light leakage phenomenon occurs when the gate voltage ( $V_g$ ) is not applied at the normally black mode. Though a black matrix is generally formed on an upper substrate (not shown) in order to intercept the light leakage in the region "A", it still may be difficult to display a high quality image if an aligning error of the upper and lower substrate occurs.

Please replace paragraph [0025] with the following paragraph:

FIG. 5 is a plan view of a pixel of an array substrate for an in-plane switching (IPS) mode liquid crystal display (LCD) device according to a first embodiment of the present invention. In FIG. 5, a plurality of gate lines 112, common lines 116 and data lines 124 are formed on an array substrate 100 for in-plane switching (IPS) mode liquid crystal display (LCD) device. The gate line 112 and the common line 116 are formed in a horizontal direction and spaced apart from each other. The data line 124 crosses the gate line 112 and the common line 116 and defines a pixel region "P" by crossing the gate line 112. A thin film transistor "T" is formed at a crossing point of the gate and data lines. The thin film transistor "T" has a gate electrode 114, an active layer 120 and source and drain electrodes 126 and 128. The gate electrode 114 communicates with the gate line 112 and the source electrode 126 communicates with the data line 124. The source electrode has an U-shape surrounding the drain electrode 128 and the drain electrode 128 has an I-shape. ~~These~~The shape of the source and drain electrodes 126 and 128 help to improve a mobility of an electron by shortening a channel length and widening a channel width between the source and drain electrodes 126 and 128. The gate electrode 114 has a slope of over about ninety degrees. A pixel electrode 130 and a common electrode 117 are formed in the pixel region "P". The pixel electrode 130 communicates with the drain electrode 128. The common electrode 117 communicates with the common line 116. The pixel electrode 130 has an extension portion 130a, a plurality of vertical portions 130b and a horizontal portion 130c. The extension portion 130a is extended from the drain electrode 128.

The vertical portions 130b are vertically extended from the extended portion 130a and spaced apart from each other. The horizontal portion 130c is disposed over the common line 116 and connects the plurality of vertical portions 130b into one portion. The common electrode 117 has a plurality of vertical portions 117b and a horizontal portion 117a. The vertical portions 117 are vertically extended from the common line 116 and arranged in an alternating pattern with the vertical portions 130b of the pixel electrode 130. The horizontal portion 117a connects the vertical portions 117b into one portion. The horizontal portion 117a of the common electrode 117 has a side that is parallel with the slope of the gate electrode 114. The slope of the gate electrode 114 is perpendicular to a rubbing direction "G". Under this structure of the common electrode and the gate electrode, an electric field direction "H" and the rubbing direction "G" become parallel to each other between the common electrode 117 and the gate electrode 114 when a gate voltage is in the off state.